Optimum High Speed and Low Power Full Adder using XNOR Cell

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Abstract –In this paper, a hybrid high energy full adder design employing both complementary metal–oxide–semiconductor (CMOS) logic is reported. The design was first implemented three transistor XNOR gate and then extended for full adder design. The circuit was implemented using Mentor Graphics software tool in 130 nm technology. A single bit full adder using eight transistors has been designed using proposed XNOR cell, which shows less power dissipation with less delay compared to normal full adder circuit..

Index Terms – CMOS, exclusive-OR (XOR), exclusive-NOR (XNOR), full adder, low power, pass transistor logic.

1. INTRODUCTION

This Increased usage of the battery-operated portable devices, like cellular phones, personal digital assistants (PDAs), and notebooks demand VLSI, and ultra large-scale integration designs with an improved power delay characteristics. Full adders, being one of the most fundamental building block of all the afore mentioned circuit applications, remain a key focus domain of the researchers over the years [1], [2]. Different logic styles, each having its own merits and bottlenecks, was investigated to implement 1-bit full adder cells [3]–[11]. There are three major source of power consumption in CMOS VLSI circuits: 1) switching power due to charging and discharging of capacitances, 2) short circuit power due to current flow from power supply to ground with simultaneous functioning of p-network and n-networks, 3) static power due to leakage currents. Binary addition is basic and most frequently used arithmetic operation in microprocessors, digital signal processors (DSP) and application-specific integrated circuits (ASIC) etc. Therefore, binary adders are crucial building blocks in VLSI circuits and efficient implementation of these adders affects the performance of entire system. The function of full adder is based on following equation, given three single bit inputs as A, B, Cin and it generates two outputs of single bit Sum and Cout, where:

$$Sum = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = A.B + C_{in}(A \oplus B) \quad (2)$$

2. RELATED WORK

In recent years various types of adder using different logic styles have been proposed. Standard CMOS 28 transistor adder using pull up and pull-down network with 14 NMOS transistors and 14 PMOS transistors is most widely reported[12]. In [13] a 16 transistors full adder cell with XOR/XNOR, pass transistor logic (PTL) and transmission gate is reported. Complementary pass-transistor logic (CPL) with 32 transistors having high power dissipation and better driving capability is reported in[14]. Full adder for embedded applications using three inputs XOR is also reported in[15]

3. PROPOSED MODELLING

The Proposed full adder circuit has been implemented by two XNOR gates and one multiplexer block as shown in block diagram of Figure 1. Sum is generated by two XNOR gates and Cout is generated by two transistors multiplexer block. The single bit full adder using proposed XNOR gates with eight transistors has been implemented and shown in Figure 5.

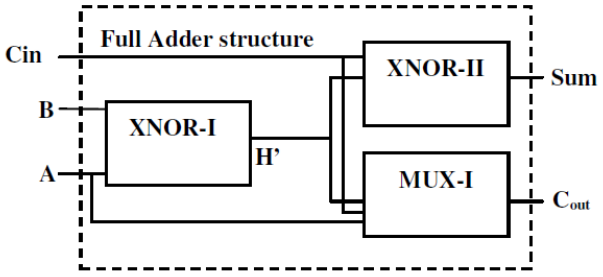


Figure 1: Schematic structure of proposed full adder.

A. XNOR *Module*

In the proposed full adder circuit, XNOR module is responsible for most of the power consumption of the entire

adder circuit. Therefore, this module is designed to minimize the power to the best possible extend with avoiding the voltage degradation possibility. Figure 2 shows the modified XNOR circuit where the power consumption is reduced significantly by deliberate use of weak inverter (channel width of transistors being small) formed by transistors. The modified XNOR presented in this paper offers low-power and high-speed (with acceptable logic swing) compared with 6 T XOR/XNOR

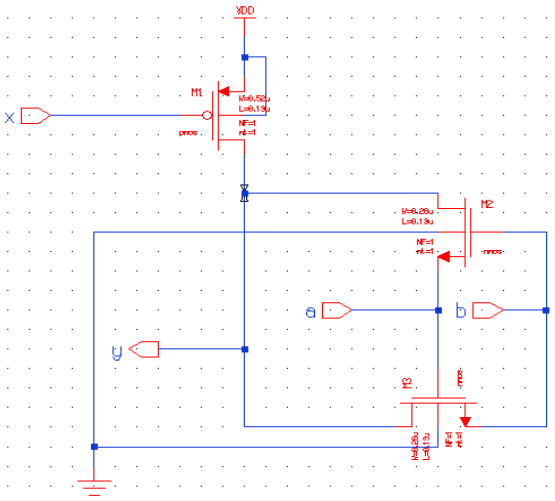


Figure 2: Three Transistors XNOR Schematic Diagram

B. Full Adder Module

Figure 3 shows the detail diagram of the proposed full adder. In previous Full adder circuit can be implemented with different combinations of XOR/XNOR modules and two multiplexers. but this approach has not been used in current work. as proposed XNOR/XOR cell shows high power consumption than single XNOR gate. Proposed full adder circuit has been implemented by two XNOR gates and one multiplexer block as shown in block diagram of Figure 1. Sum is generated by two XNOR gates and Cout is generated by two transistors multiplexer block.

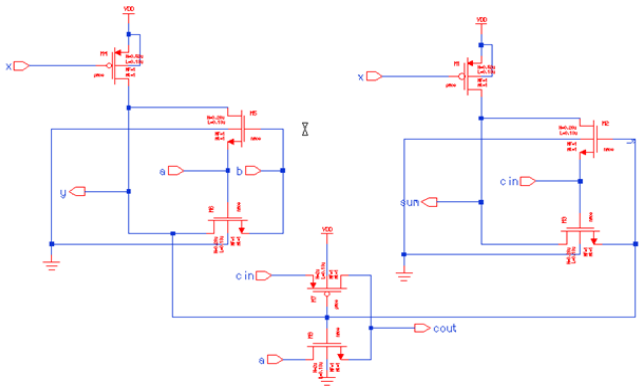


Figure 3: 8-Trasistor Full adder circuit diagram

The single bit full adder using proposed XNOR gates with eight transistors has been implemented and shown in Figure 2. For multiplexer section typical values of width (Wn & WP) 0.26µm & 0.52µm for NMOS and PMOS transistors have been taken with gate length of 0.13µm. Simulations have been performed using Mentor Graphics 130 nm technology CMOS technology with supply voltage of different voltages.

4. RESULTS AND DISCUSSIONS

Figure 4 shows the simulated block diagram for two input XNOR gate and corresponding simulated wave forms shown in figure 5. The simulated waveforms test the different logic levels and tested the simulated response.

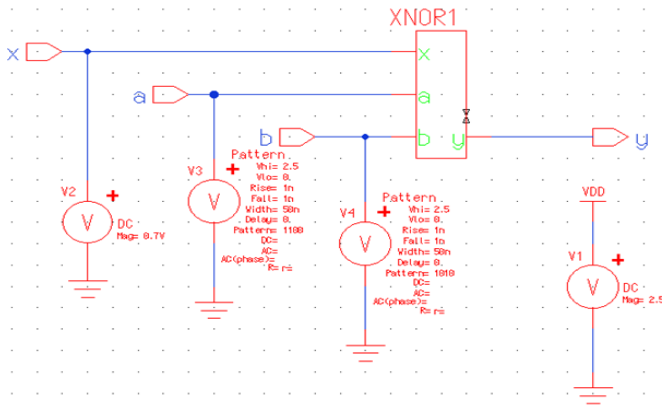


Figure 4:Simulation block diagram for XNOR gate

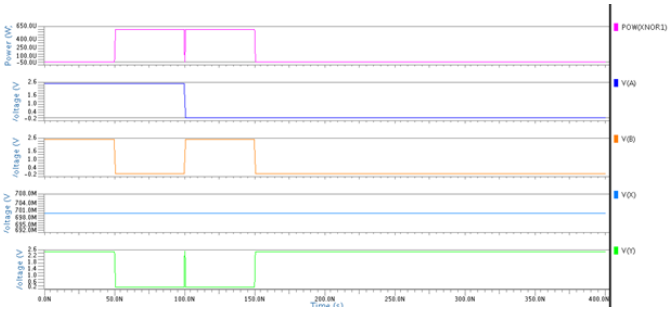


Figure 5:Simulation results for XNOR gate

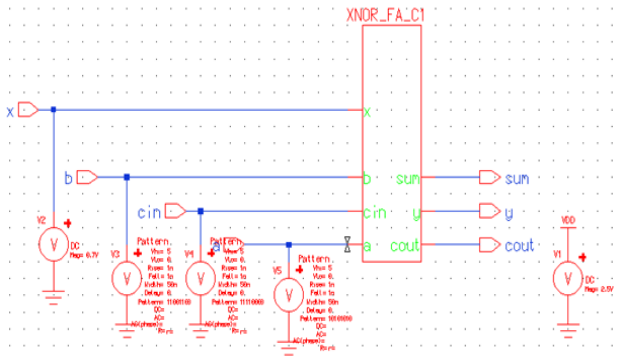
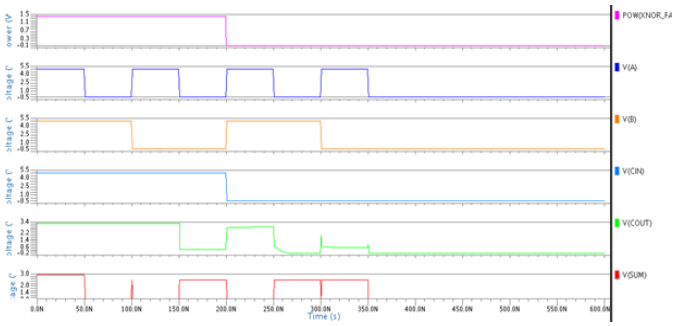


Figure 6:Simulation block diagram for 8-transistor full adder



. Figure 7:Simulation results for 8-transistor full adder

Figure 6 and figure 7 represents the simulated block and simulated wave forms for full adder for different input test cases. output response of the circuit represents the some sort of delay with respect to the applied input . Figure 8 and Figure 9 shows power dissipation and delay with 1.8V and 1.5V as the Appling voltage for XNOR and Full adder.

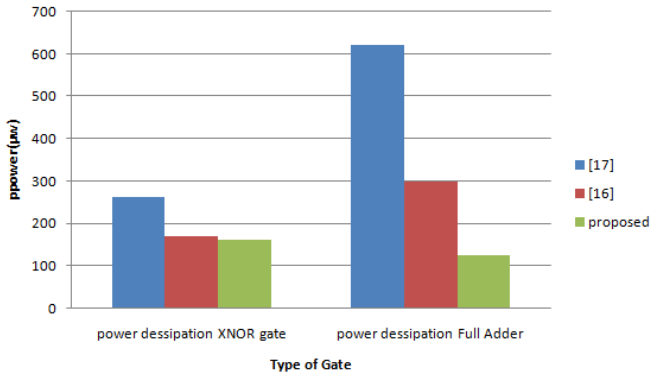


Figure 8: Comparison chart of power dissipation

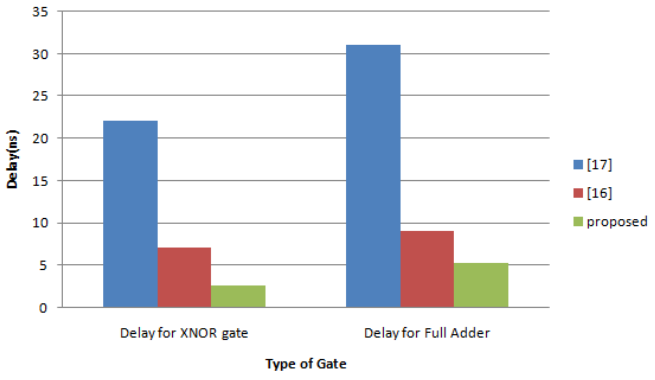


Figure 9: comparison chart of Delay

Here in proposed XNOR gate offers 160 µw of power dissipation which is very less compared to the existed methods[16],[17].it offers 2.6ns delay shows very less of 7ns and 22 ns existed delays. Using these gate impalements full adder shows the respective optimized power 124 µw dissipation and low delay 5.2 ns. in these two cases proposed methods offers 94.23% and 58.4% in power saving for XNOR and Full adder respectively. Another table II represents the power dissipation of XNOR and Full adder for different supply voltage from1V to 5V.

Supply voltage	Power dissipation(µW) (XNOR Gate)	Delay(ns) (XNOR Gate)	Power dissipation(µW) (Full Adder)
1.0	1.0365	--------	30.626
1.5	57.487	0.0214	124.0.5
1.8	160.48	2.46	325.98
2.5	595.53	2.86	698.33
5.0	4.52e+12	3.50	12.494

Table 2: Power dissipation & Delay outputs for XNOR and Full adder for supply voltages varying for 1v to 5v

5. CONCLUSION

In this paper we proposed an XNOR gate using 3 transistors and 8 transistors Full adder EDA tool at 130nm technology. From the results and comparison table, it is concluded that the design proposed for XNOR gate using 3 transistors, full adder using 8 transistors has better performance than normal adder in terms of delay and power. By efficiently mapping into EDA tool. The results of mapping are viewed using ELDO Waves in MENTOR GRAPHICS at 130 nm technology at different voltages[1V-5V]. The pre-simulation results have been computed using 130nm technology. The previously existing XNOR gate occupied high power & large delay which has been refined in our present design. The presented 3T XNOR gate aims at emphasizing less delay & low power. From the output result i found out around 94.83% in XNOR gate and 58.3% in full adder less power is dissipated and also fast operation (less delay) is taking place by doing this process in EDA TOOL.

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